Laboratory WORK REPORT №4

« Simple digital circuits design and simulation »

**Principles of Circuits**

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# Work purpose: to study transistor switch, logic families and simple logic schemes

Goals:

1) Design transistor switch

2) Simulate transistor switch in LtSpice

3) Design simple logic scheme

4) Additional task – logic element design in LtSpice

# Starting data

### 2.1 Parameters of the voltage source:

2.2 Transistor type – FZT849

# Transistor switch mode

3.1 Parameters of scheme element (with calculations)

3.1.1 Collector current you choose 7 A

3.1.2 Collector resistor value

0.664 Ω

3.1.3 Base current (minimum value)

0.047 A

3.1.4 Saturation base current you choose = 0.047 A

3.1.5 Base resistor value

=80.85 Ω

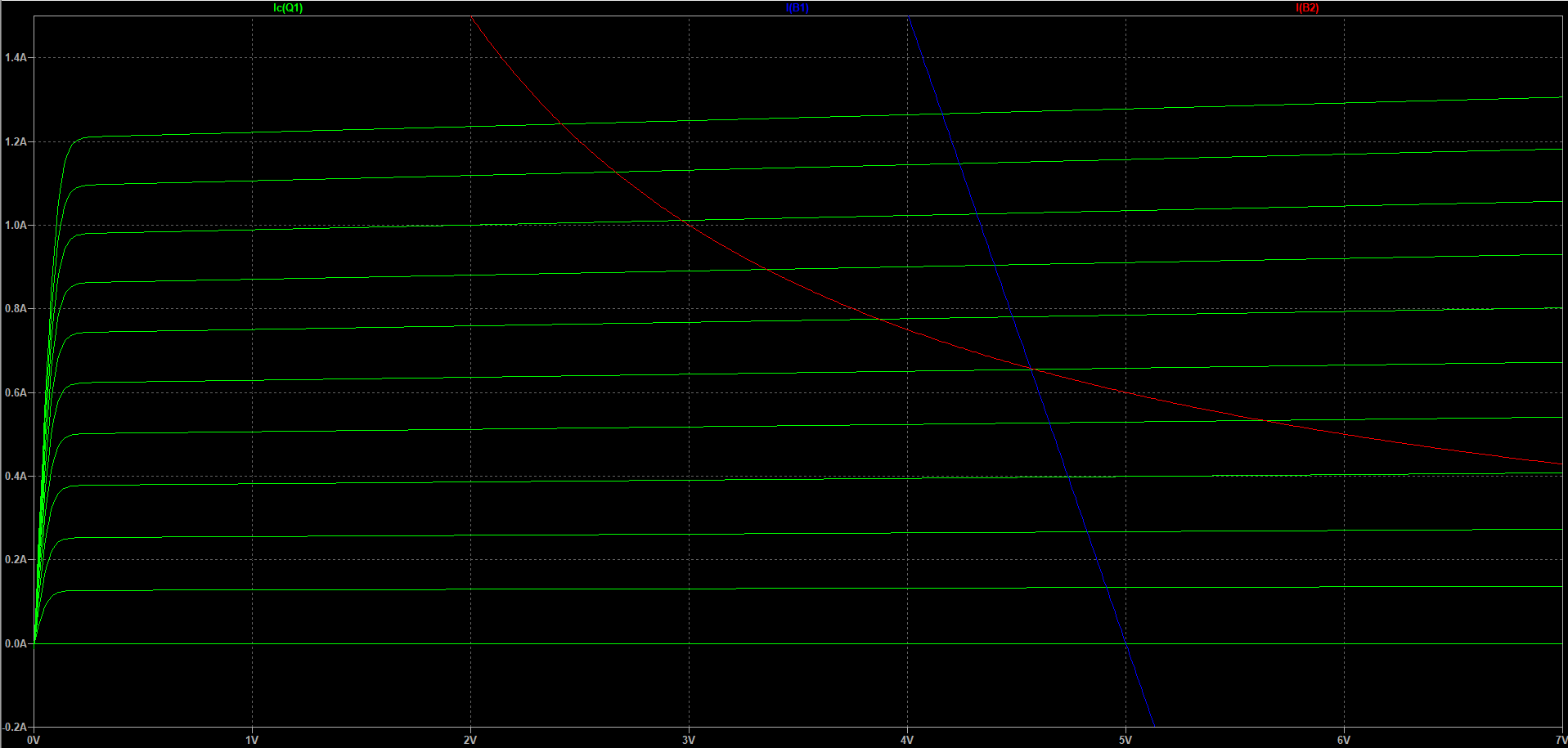


Fig. 1 – Output volt-ampere characteristic

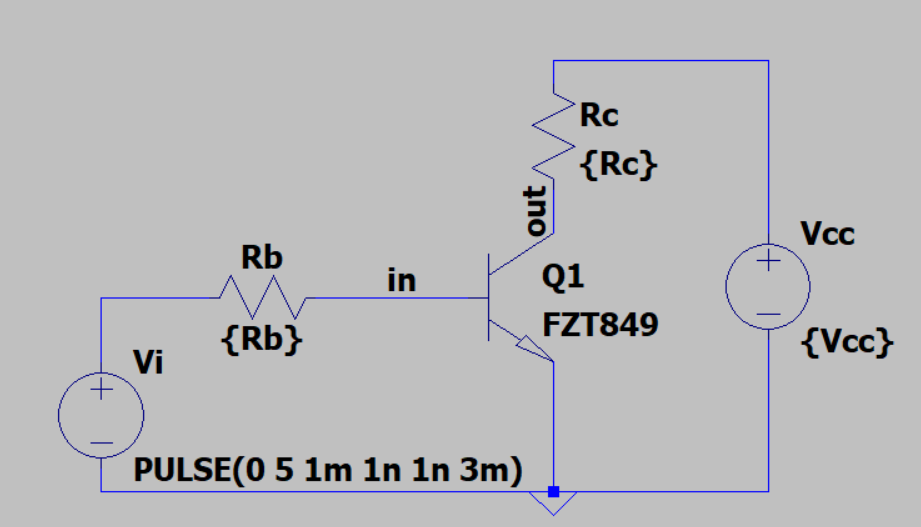


Fig.2 - Inverter circuit

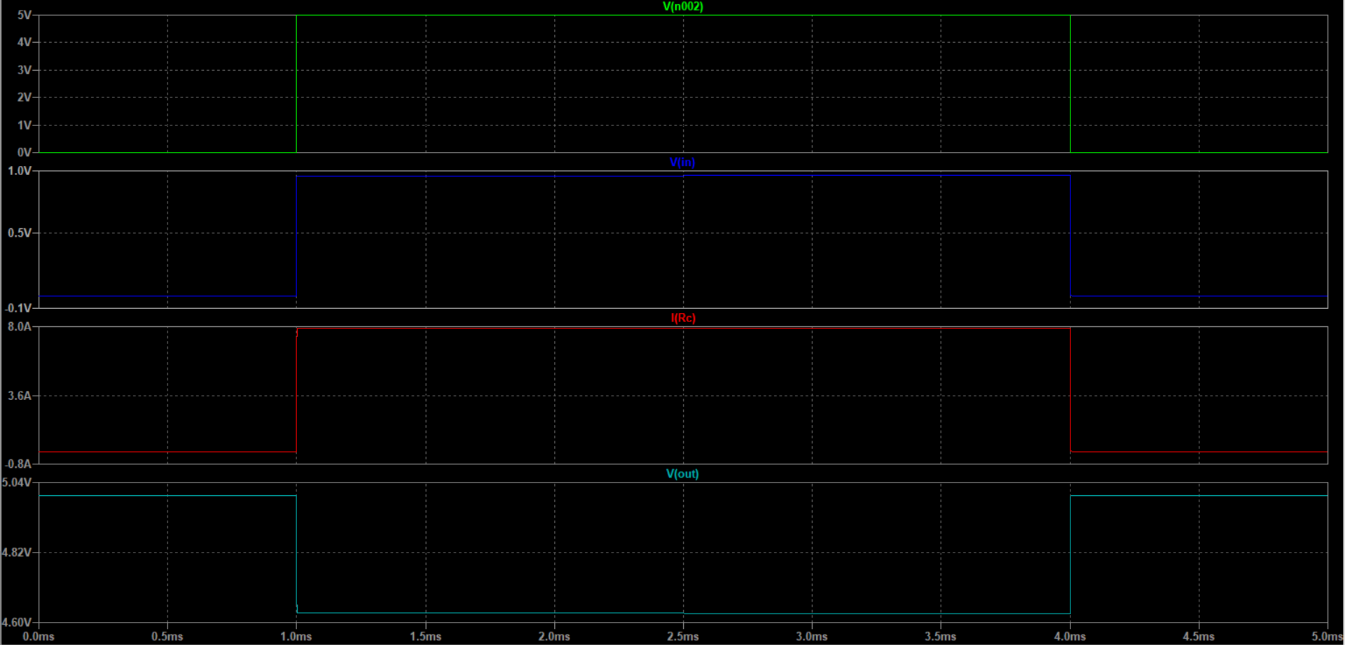


Fig. 3 – Time diagram for BJT switch

**Conclusions** on the first part of the laboratory work - We set different parameters according to different triode models.

# Combinational Logic Circuits

The combination logic circuit and true table are shown on figure 4.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| № | A | B | C | D | Y |
| 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 1 | 1 | 1 | 1 |
| 3 | 1 | 0 | 1 | 1 | 1 |
| 4 | 0 | 0 | 1 | 1 | 1 |
| 5 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 0 | 1 | 1 |
| 7 | 1 | 0 | 0 | 1 | 1 |
| 8 | 0 | 0 | 0 | 1 | 1 |
| 9 | 1 | 1 | 1 | 0 | 1 |
| 10 | 0 | 1 | 1 | 0 | 1 |
| 11 | 1 | 0 | 1 | 0 | 1 |
| 12 | 0 | 0 | 1 | 0 | 1 |
| 13 | 1 | 1 | 0 | 0 | 1 |
| 14 | 0 | 1 | 0 | 0 | 1 |
| 15 | 1 | 0 | 0 | 0 | 1 |
| 16 | 0 | 0 | 0 | 0 | 0 |

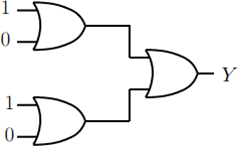


Fig. 4 - The combination logic circuit and true table

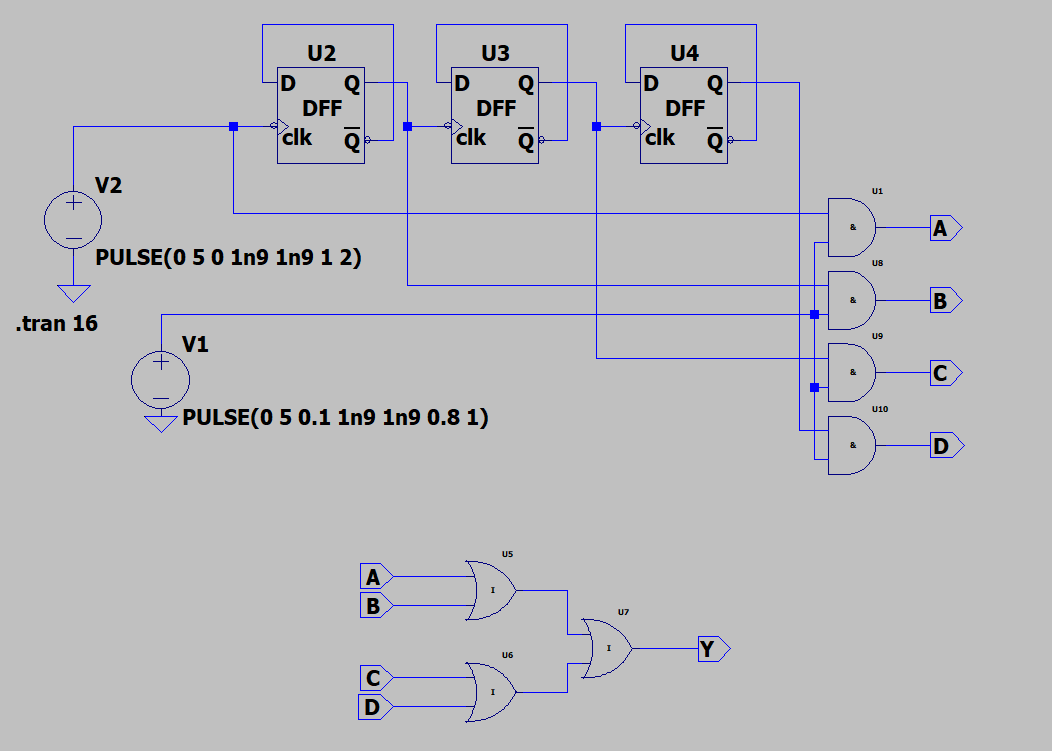


Fig.5 – Simulation model from LtSpice

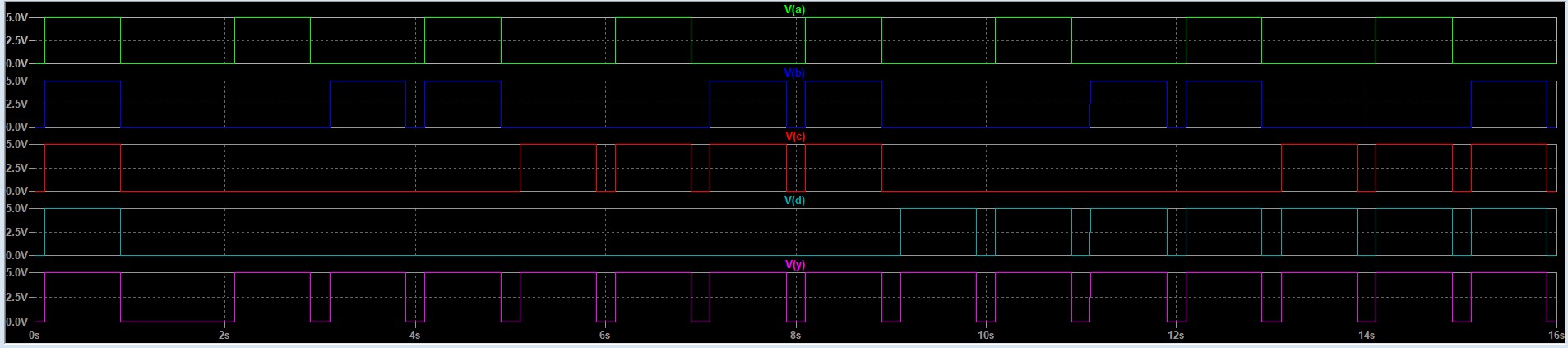


Fig. 6 – Simulation results

**Conclusions** on the second part of the laboratory work - We judge the truth table corresponding to the logic gate according to the output waveform.

# Logic families

Logic element is shown in fig. 7.

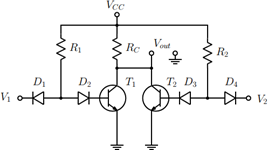


Fig. 7 – Logic element scheme and true table

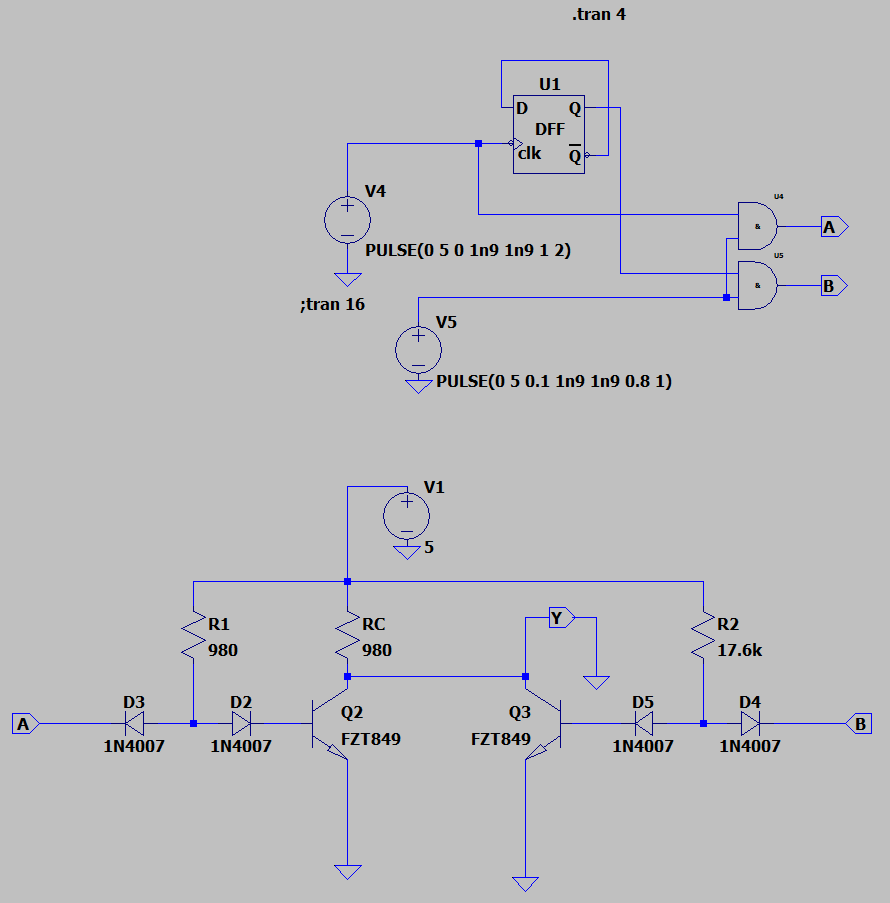


Fig. 8 – Simulation model from LtSpice

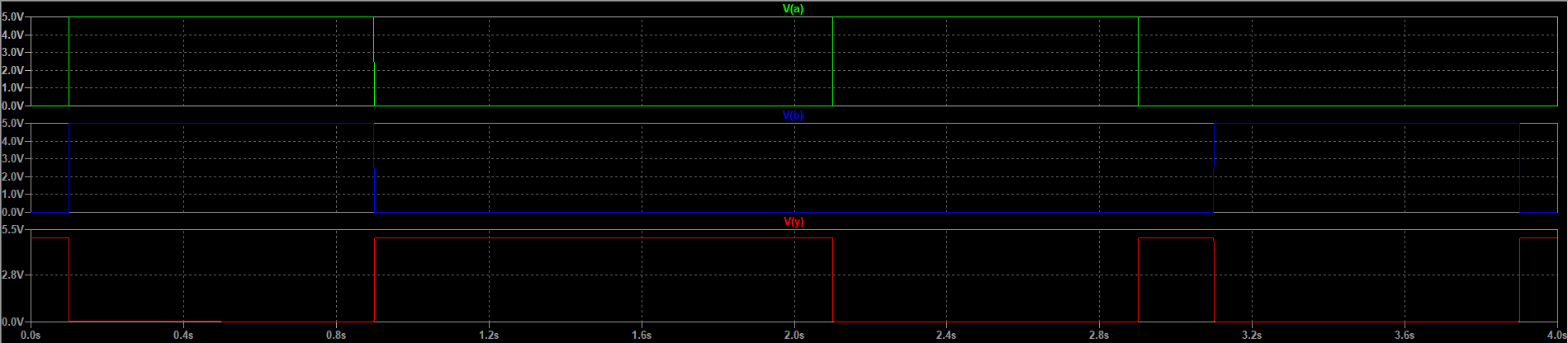


Fig. 9 – Simulation results

**Conclusions** on the third part of the laboratory work - We drew the corresponding logic circuit and recorded its output results.